

Attorney Docket #10010586

Amendments to the Claims

This list of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-11 (canceled)

12. (currently amended) A wafer-level package, comprising:

a first semiconductor wafer having an elevated portion and an etched lower surface, wherein the elevated portion has a flat surface original to the semiconductor wafer and surrounds an area of the etched lower surface; and

a device fabricated on the first semiconductor wafer;

a second semiconductor wafer;

~~a gasket formed from the first wafer;~~

a pad on the second semiconductor wafer, substantially matching the ~~gasket~~ elevated portion; and

bonding material joining the ~~gasket~~ the elevated portion and the pad to enclose the device within a hermetically sealed environment between the first and second semiconductor wafers.

13. (original) The wafer-level package of claim 12 wherein the first wafer is formed of silicon.

14. (currently amended) The wafer-level package of claim 13 wherein the elevated portion gasket is no more than 20 μm wide.

15. (currently amended) The wafer-level package of claim 14 wherein the elevated portion gasket is no more than 10 μm wide.

16. (original) The wafer-level package of claim 14 wherein the bonding material includes conductive bonding material.

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17. (original) The wafer-level package of claim 16 wherein the conductive bonding material is a metal selected from the group consisting of gold, gold-tin, tin-lead, and palladium-tin.

18. (original) The wafer-level package of claim 14 wherein the bonding material includes non-conductive bonding material.

19. (original) The wafer-level package of claim 18 wherein the non-conductive bonding material is a material selected from the group consisting of polyimide, B-staged bisbenzocyclobutene (BCB), and glass.

20. (currently amended) A wafer-level package, comprising:

a first semiconductor wafer having an elevated portion and an etched lower surface, wherein the elevated portion has a flat surface original to the semiconductor wafer and surrounds an area of the etched lower surface; and

a device fabricated on the first semiconductor wafer;

a second semiconductor wafer;

a gasket formed from the first wafer;

bonding material joining the gasket the elevated portion and the second semiconductor wafer to enclose the device within a hermetically sealed environment between the first and second semiconductor wafers..

21. (currently amended) The wafer-level package of claim 20, wherein the elevated portion gasket is less than 20 μm wide.

22. (currently amended) The wafer-level package of claim 21, wherein the elevated portion is less than 10 μm wide.

23. (original) The wafer-level package of claim 21, wherein the bonding material is non-conductive.

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24. (original) The wafer-level package of claim 23, wherein the non-conductive bonding material is selected from the group consisting of polyimide, B-staged bisbenzocyclobutene (BCB), and glass.